Dennis **Potter**

Electrical Engineer · Computer Engineer

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Summary

I am a senior staff engineer digital IC design at Marvell Semiconductor and have always been curious about technological innovations. For that reason I graduated in electrical engineering, information technology & computer engineering. I have always striven for a complete understanding of computers, from the lowest level—i.e., the bare integrated circuits—to the highest—i.e., user space—and am therefore always eager to learn something new. I enjoy writing small programs in my free time, either to automate everyday problems, or simply for the sake of fun, and get excited by the seemingly endless possibilities of Linux. Furthermore, there is always time for a good read, also on non-tech subjects like economics, anthropology, or (geo)politics.

Skills

Programming & Scripting	SystemVerilog, C, C++, Python, Rust, SystemC, Perl, TCL, Make, Bash, TCSH, MATLAB
Markup languages	HTML5, CSS, LaTeX, Markdown
Miscellaneous	Ethernet, MACsec, PTP, CSI2, RISC-V, Infiniband, Linux
Languages	Dutch, English, German

Work Experience

Marvell Semiconductor

Senior Staff Digital Design Engineer — *Jul. 2021 - Present // Santa Clara (USA)*

- Owning a digital subsystem that provides MACsec (IEEE 802.3AE), PTP (IEEE 1588/IEEE 802.1AS), and MAC functionalities.
- Maintaining & improving the proprietary Logic Analyser Module (LAM) hardware and software. Debugging silicon issues on various products with help of the proprietary LAM.
- Improving & extending the previously designed front-end methodology. This includes, i.a., replacing underperforming EDA tools, using novel version control management techniques to improve user usability & efficiency, adding automated regression tests to increase the (early) detection of bugs.
- Reviewing digital signal processing (DSP) hardware in a coherent optical DSP chip and developing the firmware for said hardware.

Marvell Semiconductor

Staff Digital Design Engineer — *Oct. 2019 - Jul. 2021 // Aachen (D)*

- Owning a digital subsystem that provides MACsec (IEEE 802.3AE), PTP (IEEE 1588/IEEE 802.1AS), and MAC functionalities.
- Co-architecting and implementing a CSI module. This includes the encapsulation of pseudo-CSI2-packets into Ethernet packets with a configurable Ethernet/IP/UDP/AVTP header at the Rx-side of the block, and decapsulation and reordering of those packets at a Tx-side.
- Creating software to extract signals from a proprietary Logic Analyser Module and subsequently translating it to a VCD file that can be interpreted by any waveform viewer.
- Developing a script to automatically resolve congestion issues and Lint warnings in auto-generated register files.
- Debugging AHB bus issues in full chip simulations.
- Setting up a methodology for all front-end activity. This includes, i.a., the directory structure, version control management, regression management, RTL coding guidelines, and design libraries. Furthermore, convenient wrapper scripts that seemingly integrate in the flow for Cadence Joules, Spyglass Lint, Mentor CDC, Agnisys idsbatch, Cadence Conformal, and TSMC memories were written.

Aquantia Corp.

Member of Technical Staff II — *Dec. 2018 - Sept. 2019 // Aachen (D)*

- Designing a store & forward Ethernet switch with a dynamic CAM, FRER (de)duplication, and seperate lanes for high- and low priority traffic.
- Creating a proprietary Logic Analyser Module to extract signals from the silicon chip. This includes cyclic buffering, triggering on (maskable) patterns, filtering (maskable) patterns, and compression.
- Developing a Python script to pre-process (hierarchical) Verilog Manifest files and sanity checking the included files.

Contractor — *Aug. 2017 - Nov. 2018 // Aachen (D)*

- Developing a synthesizable layer 2 Ethernet switch in SystemC and evaluating DV & synthesis capabilities of a high-level synthesis suite.
- Providing support for the FPGA GUI and the power analysis environment that was developed during the internship.

Intern — *Nov. 2016 - July. 2017 // San José (USA)*

- RTL power analysis and reduction on various digital designs using Ansys' PowerArtist.
- Developing an intuitive GUI—written in Python, Tkinter, and C—to control an FPGA Ethernet debug tool.

Boscafé 't Hijgend Hert

Web developer and server administrator — *Apr. 2012 - Mar. 2018 // Vijlen (NL)*

- Boscafé 't Hijgend Hert is a popular restaurant (500+ seats) & tourist destination in the south of the Netherlands. Responsibilities included the restaurant's IT (including POS systems), the development of several websites, and the maintenance and security of their Linux based VPS.

Chair for Electrical Engineering and Computer Systems, RWTH Aachen University

Student Research Assistent — *May. 2016 - July. 2016 // Aachen (D)*

- Establishment of burst-mode communication between the FPGA fabric and CPU subsystem, over AXI and/or DDR interface on Altera Cyclone V devices.

Education

RWTH Aachen University

M.Sc. Electrical Engineering, Information Technology, & Computer Engineering — *Oct. 2015 - Nov. 2018 // Aachen (D)*

- *Specialization*: Micro- and Nanoelectronics
- *Final project*: "Implementation and Analysis of RDMA Communication in a Real-Time Co-Simulation Framework"—An analysis and subsequent implementation of the Virtual Interface Architecture Infiniband, using the OpenStack verbs, in order to achieve high throughput and minimal latency between nodes of the real-time co-simulation framework VILLASnode.
- *Modules included*: lectures on VLSI architectures, computer arithmetics, mixed analog signals, neural networks, new materials and devices in information technology, numerical device simulation, and operating systems. Lab trainings on full custom design, FPGA development, and on the production of FeRAM cells.

B.Sc. Electrical Engineering, Information Technology, & Computer Engineering — *Oct. 2011 - Sept. 2015 // Aachen (D)*

- *Final project*: "Analysis of Concepts for Power Reduction in Arithmetic Units of MAP Decoders"—A mathematical, bit accurate implementation of a decoder in MATLAB and C++, to find techniques that will potentially reduce the switching activity (and thus the power) in the arithmetic units of the decoder.

Sophianum SG. in het Heuvelland

Gymnasium (Comparable to a university-preparatory school with Latin as additional language.) — *Sept. 2005 - July. 2011 // Gulpen (NL)*